



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.: 10/602,194
Applicant: Yoshi Ono
Filed: June 23, 2003
Group #: 2823
Examiner: Khiem D. Nguyen

Confirmation Number: 9996

Docket No: SLA.0669
Customer No: 55376
For: Low Temperature Nitridation of Silicon

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

**TRANSMITTAL OF
NOTICE OF APPEAL
PRE-APPEAL BRIEF REQUEST FOR REVIEW**

Applicants submit the following:

1. Notice of Appeal
2. Pre-Appeal Brief Request for Review
3. Attachment to Pre-Appeal Brief Request for Review
4. PTOForm 2038 in the amount of \$500.00 as the Notice of Appeal Fee

Provisional Request for Extension of time in Which to Respond

Should this response be deemed to be untimely, Applicants hereby request an extension of time under 37 C.F.R. § 1.136. The Commissioner is hereby authorized to charge

any additional fees which may be required, or credit any over-payment to Account No. 22-0258.

Customer Number

55376

Respectfully Submitted,

ROBERT D. VARITZ, P.C.

Registration No: 31436

Telephone: 503-720-1983

Facsimile: 503-233-7730


Robert D. Varitz

4915 S.E. 33d Place

Portland, Oregon 97202

CERTIFICATE OF EXPRESS MAILING

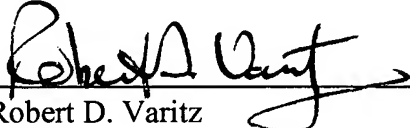
"Express Mail" Mailing Label No.

Date of Deposit - April 6, 2006

EV756095365US)

I hereby certify that the attached Notice of Appeal, Pre-Appeal Brief Request for Review, Attachment to Pre-Appeal Brief Request for Review, and PTO Form 2038 in the amount of \$500.00 as the Notice of Appeal Fee are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to:

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Washington, D.C. 22313-1450


Robert D. Varitz



Doc Code: AP.PRE.REQ

PTO/SB/33 (07-05)

Approved for use through xx/xx/200x. OMB 0651-00xx

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)

SLA.0669

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as ~~EXPRESS~~ in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on April 6, 2006

Signature

Typed or printed name

Robert D. Varitz

Application Number

10/602,194

Filed

06/23/2003

First Named Inventor

Yoshi Ono

Art Unit

2823

Examiner

Khien D. Nguyen

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

☐

applicant/inventor.

☐

assignee of record of the entire interest.

See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☒

attorney or agent of record.

Registration number 31436☐

attorney or agent acting under 37 CFR 1.34.

Registration number if acting under 37 CFR 1.34 _____

Signature

Robert D. Varitz

Typed or printed name

503-720-1983

Telephone number

April 6, 2006

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒*Total of -1- forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

In the Office action dated January 10, 2006, the Examiner finally rejected all claims under 35 U.S.C. § 103(a) as being unpatentable over U. S. Patent No. 4,495,218 of Azuma *et al.*

The Invention

The invention is a method of forming a high quality silicon nitride layer at low temperature in an integrated circuit. The method of the invention employs the use of nitrogen radicals to convert silicon to a silicon nitride, thus *growing* a silicon nitride thin film on a silicon-containing layer. The method of the invention may also form a thin nitride layer on an already-grown silicon oxide layer by displacing the oxygen at the top surface and converting at least a portion of silicon oxide to silicon nitride. The method of the invention does not use a plasma discharge, which may cause substantial damage to the silicon wafer, nor does the method of the invention require the use of a silane gas. The method of the invention generates large quantities of nitrogen radicals on or near the surface of a silicon layer, or silicon oxide layer, which is to be converted to silicon nitride. The radicals are generated by the photolysis, or photo-dissociation, of NH_3 . The light source used is a Xe_2 excimer lamp which emits at a wavelength of 172 nm, or 7.21eV in energy. The direct illumination of the wafer surface at such an energy level may generate photoelectrons and a charged surface that may participate in the nitridation process. The work function of silicon is less than 5eV, so electrons can have over 2.2eV of kinetic energy. Electron attachment of the low energy electrons may generate negatively charged species, such as NH_2^- , that are quite stable. Adsorbed molecules on the surface of the substrate may also play a role in the nitride layer growth. The growth of the film may be assisted by a field across the growing dielectric layer where a positively charged interface attracts negative ions.

The Applied Art

The Examiner has applied a single reference under 35 U.S.C. § 103(a): U. S. Patent No. 4,495,218 of Azuma *et al.* for *Process for forming thin film*, granted January 22, 1985. The '218 patent teaches that a thin film may be deposited on a substrate by introduction of the components of the final thin film in gaseous form into a CVD chamber, *e.g.*, a nitrogen-containing gas and a silicon-containing gas are introduced into the CVD chamber..

The Claims

The independent claims recite that the silicon nitride thin film of the method of the invention is *grown* on the substrate. Those of ordinary skill in the art will appreciate that there is a difference between depositing a layer of material and growing a layer of material: the method of the invention grows the silicon nitride layer from a combination of gaseous nitrogen and silicon present in or on the substrate. Whether the silicon on the substrate is in pure form or part of a silicon oxide layer is irrelevant to the method of the invention. '218 teaches, in the portions applied by the Examiner, col. 3, lines 11-39, that silicon is introduced into a CVD chamber in the form of a silane compound in gaseous form, and that the '218 method of the invention may be used to deposit a layer of a-silicon, silicon oxide or silicon nitride by thermal and plasma CVD methods. Applicant specifically teaches away from plasma CVD because such process actually damages the silicon layer, Specification, page 3, lines 15-18.

Claims 1, 9 and 16 are allowable over the applied art because the applied art does not teach or suggest formation of a silicon nitride layer wherein the silicon of the silicon nitride layer is obtained from a silicon-containing substrate; the '218 reference, like all of the other applied references in the long history of this Application, teaches that silicon is introduced into a

CVD chamber in a silicon-containing gas form with a nitrogen-containing gas, which results in deposition of a silicon nitride layer. This is not what Applicant teach or claims.

The Examiner has failed to establish a *prima facie* case to support his rejection of the claims because the applied art neither teaches nor suggests the method of the invention disclosed by Applicant. For the applied art to teach or suggest the method of the invention, the use of a silicon-containing gas must be omitted. There is no suggestion anywhere in '218 that this happen. Were one to use the method of '218 without the use of a silicon-containing gas, the method of the invention of '218 would become inoperable. For this reason, the claims, as now present in the Application, are allowable over the applied art of record.